ABSTRACT

[32] Method and system for translating Verilog to C++ are provided herein. Aspects of the method for translating may include searching for a Verilog pattern in a Verilog file and substituting the Verilog pattern with a C++ language expression, wherein the C++ language expression is associated with the same functionality as the Verilog pattern. It may be identified whether the Verilog file comprises at least one of a task library, a main driver, and a driver module. If the Verilog file comprises a task library, a Verilog task within the task library may be identified; and the Verilog task may be translated into a C++ function. If the Verilog file comprises a main driver, a C++ interface header may be inserted in the Verilog file.